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## UV Sensor

# YL-2023F-UVADS(A)

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### FEATURES

- UVA sensing with 16-bit resolution
- Support UV index measurement (0~16)
- Programmable gain and integration time
- I<sup>2</sup>C slave interface up to 400KHz
- Power management modes
- Shutdown current : 0.8uA typical
- Supply voltage of 2.2V to 3.6V
- 2.0mm×2.3mm×1.4mm ,4-pin COBpackage

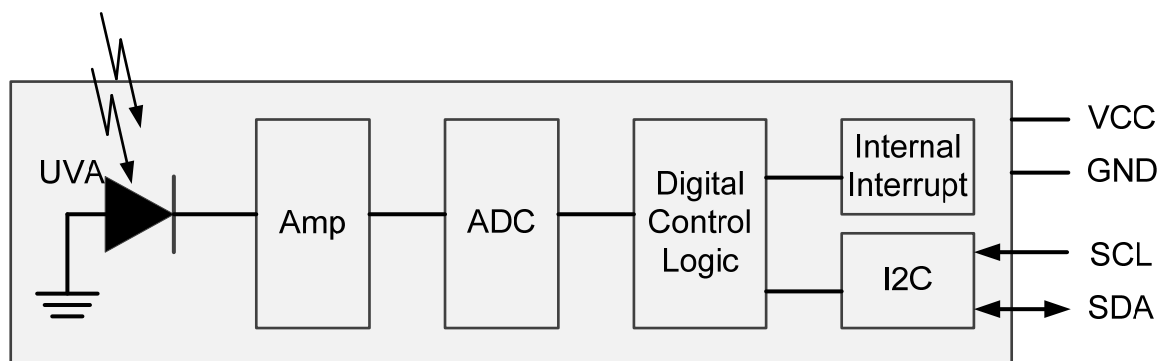
### GENERAL DESCRIPTION

YL-2023F-UVADS(A) supports integrated functions of ultraviolet light sensors such that can be easily configured and used in user applications. YL-2023F-UVADS(A) comprises photodiodes, amplifiers, ADC, digital control logic and I<sup>2</sup>C interface circuit. YL-2023F-UVADS(A) receives UVA and outputs digital count according to the intensity. Power consumption can be minimized by proper use of power management mode.

### APPLICATIONS

Smartphone, Wearable devices, IoT, watch, weather station, bicycle navigation, gaming, accessory

### FUNCTIONAL BLOCK DIAGRAM



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## 1. SPECIFICATIONS

Unless otherwise noted, all the measurement results are based on  $T_A=25^{\circ}\text{C}$  and  $V_{CC}=3.0\text{V}$ . Typical specifications are not guaranteed while all the minimum and maximum specifications are guaranteed.

**Table 1.1 Electrical characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>Functional</b>						
$V_{CC}$	Power supply voltage		2.2	3.0	3.6	V
$V_{OH}$	High-level output voltage		1.22			V
$V_{OL}$	Low-level output voltage				0.4	V
$V_{IH}$	High-level input voltage		$0.8 * V_{CC}$			V
$V_{IL}$	Low-level input voltage				$0.2 * V_{CC}$	V
$I_{DD}$	Current consumption	Normal mode		150	160	$\mu\text{A}$
$I_{DS}$		Shutdown mode		0.8	1	
$F_{I2C}$	I <sup>2</sup> C clock frequency		1		400	kHz
$T_{ADC}$	ADC conversion time	RES=011(100ms)	95	100	105	ms
$ADC_f$	Full scale ADC code	RES =011(100ms)			65535	LSB
$ADC_d$	ADC code for dark current	RES =011, RANGE UVA = 011,		0	3	LSB
$T_{OP}$	Operating temperature		-30		85	$^{\circ}\text{C}$
<b>UVA</b>						
	Wavelength		240		370	nm
$I_{PH}$	Photo Current	352nm UVA 4W Lamp,		23.94		nA
$ADC_{UVA}$	ADC code for UVA	352nm UVA 4W Lamp,		TBD		LSB

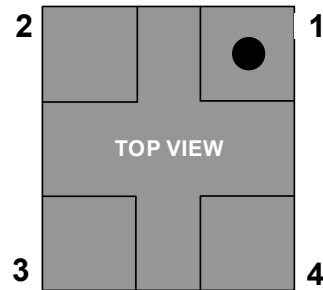
## 2. ABSOLUTE MAXIMUM RATINGS

Stresses above these listed absolute maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect the device reliability or cause malfunction.

**Table 2.1 Absolute Maximum ratings**

Symbol	Parameter	Min	Max	Units
V <sub>CC</sub>	Power supply voltage	-0.3	3.6	V
V <sub>IO</sub>	Digital I/O signal voltage	-0.3	3.6	V
ESD	HBM		2	kV
	CDM		700	V
T <sub>OP</sub>	Operating temperature	-30	+85	°C
T <sub>STORE</sub>	Storage temperature range	-40	+85	°C
T <sub>SOLDER</sub>	Soldering temperature (peak temperature duration: 10s)		260	°C

### 3. PIN CONFIGURATION AND DESCRIPTION



2mm x 2.3mm COB package (1.4mm thickness)

Figure 3.1 Pin configurations (Top view)

Table 3.1 Pin description

Pin #	Name	I/O Type	Description
1	GND	Ground	Ground
2	SDA	Digital in/out	I <sup>2</sup> C data line
3	SCL	Digital input	I <sup>2</sup> C clock line
4	VCC	Supply	Supply voltage

4. PACKAGE INFORMATION

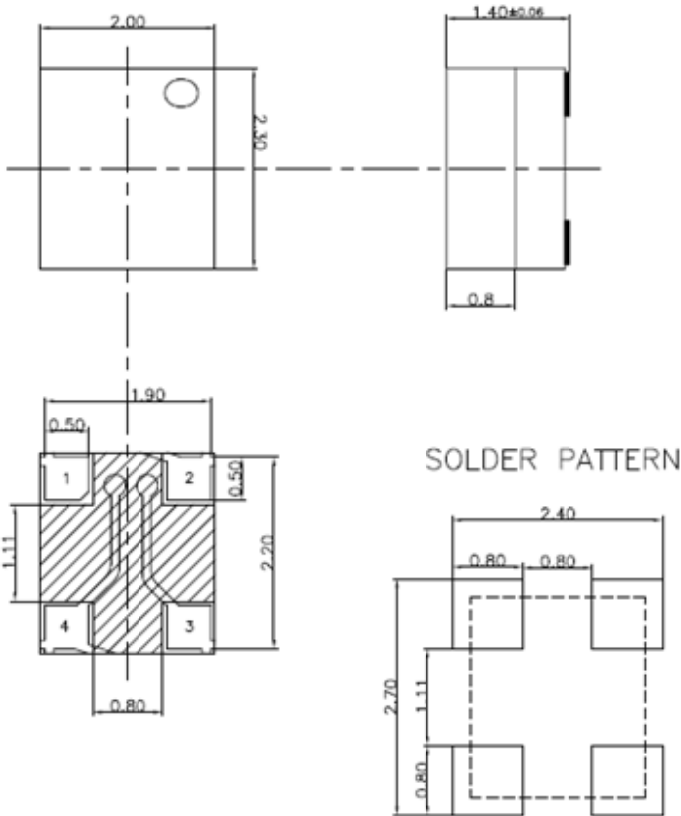
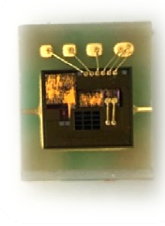


Figure 4.1 Package outline dimension

## 5. APPLICATION CIRCUITS

$C_{VCC}$  is used to reduce the power supply noise, and also should be placed near pin 4. For the I<sup>2</sup>C operation, SDA and SCL need pull-up resistors. The recommended component values are in Table 5.1.

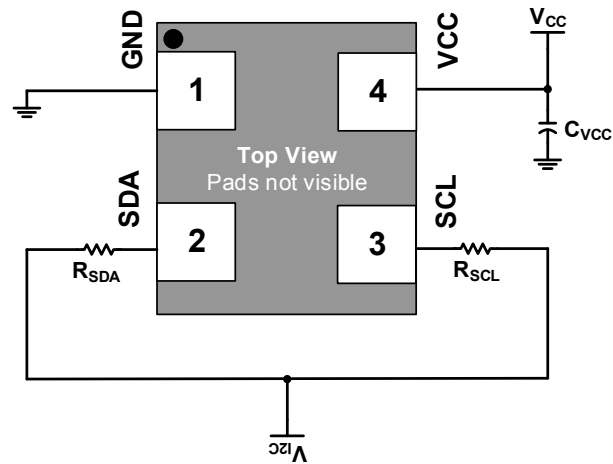


Figure 5.1 Application circuit

Table 5.1 Recommended values

Components	Recommended values
$C_{VCC}$	1uF
$R_{SCL}$	4.7k $\Omega$
$R_{SDA}$	4.7k $\Omega$

## 6. FUNCTIONAL DESCRIPTION

YL-2023F-UVADS(A) is an integrated circuit of an UVA sensor and ROIC. It includes on-chip photodiodes, ADCs, amplifiers, comparators and I<sup>2</sup>C interface. The photo detectors sense the amount of incident light for the UVA. The current generated by photo detectors is converted and measured by ADC and changed to 16-bit resolution digital data. The measured data can be delivered to host CPU via I<sup>2</sup>C serial interface. YL-2023F-UVADS(A) can internally generate the interrupt signal to reduce the burden of host CPU by informing the occurrence of specified events.

Communication with host CPU is accomplished through I<sup>2</sup>C serial interface. The fastest speed of the interface is 400kHz.

### SYSTEM RESET

System reset circuit is shown in Figure 6.1. When the system reset signal is generated, all the internal registers are initialized. System reset signal is generated from either POR (power-on-reset) circuit or SoftReset signal. POR circuit releases reset signal when VDD signal rises to the specified voltage after power up. The SoftReset signal is generated when host CPU writes 0xA5 value to the register of address 0x0B.

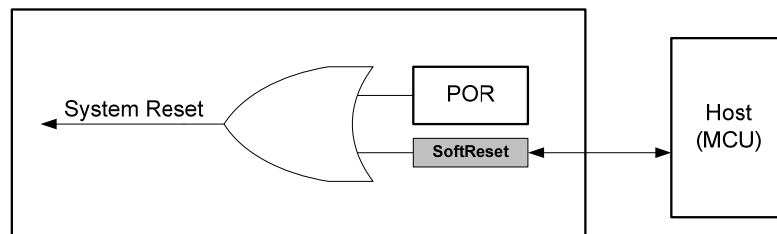


Figure 6.1. System reset circuit

### POWER MANAGEMENT MODES

YL-2023F-UVADS(A) supports 4 power management modes to save power consumption;

- normal mode
- low-power mode
- auto-shutdown mode
- shutdown mode

As soon as power is up, YL-2023F-UVADS(A) enters into shutdown mode. In normal mode, the amount of UVA is repetitively measured according to the value of OPER field. In low-power mode, all the other circuits except system management and host interface circuits are periodically deactivated to save power consumption.

The power consumption is minimized in shutdown mode as all the circuits except host interface are disabled. In auto-shutdown mode, UVA sensing operation is executed just once

and behave as shutdown mode afterwards. The power management mode can be selected by PMODE[1:0] field of MODE register at address 0x01.

### UVA SENSING OPERATIONS

In other modes except shutdown mode, the sensing operation can be set as follows;

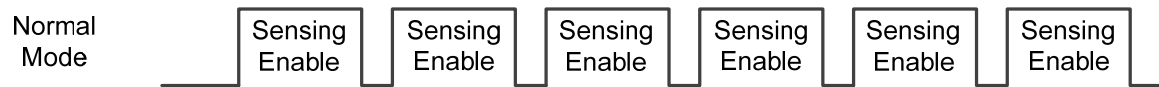
In UVA operation, the photodiode for UVA is used to detect the amount of incident light. The measured data is output to UVA registers at address 0x15 and 0x16.

The sensing operations are selected by the value of OPER field of MODE register at address 0x01.

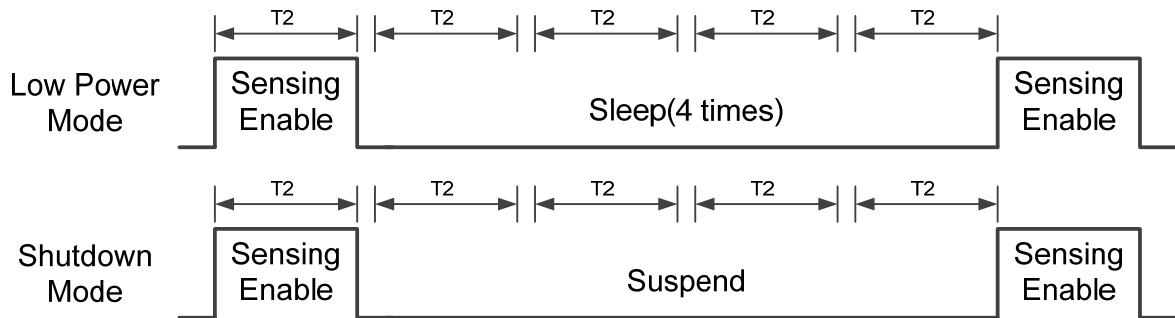
Figure 6.2 shows the possible sensing operations in the normal mode. Figure 6.3 shows the low-power and auto-shutdown mode operations. The sleep duration is



controlled by SLP\_PER[1:0] field of MODE\_CTL register at address 0x0A.



**Figure 6.2. Normal mode operations**



**Figure 6.3. Low-power and shutdown mode operations**

## RESOLUTION AND RANGE

Resolution defines how finely the incident light can be measured. And it is proportional to ADC measuring time. If the ADC measuring time is increased by 2 times, the resolution can be increased by 1 bit.

The resolution for sensor is selected by RES[2:0] field of RES register at address 0x04. The default resolution is 16 bits and the measuring time is 100ms.

In sensing operation, if the resolution is over 16 bits, the upper 16 bits of the measured result is output as measured data.

Range controls the range of intensity of the incident light. In the case of incident light

exceeding the full range(in other words, overflow), the maximum value of sensor is output as measured data. That is, the exact measured data can't be obtained. The range can be changed in order that the measured data is represented in the maximum value.

The range for sensor is selected by RANGE[2:0] field of RANGE register at address 0x05.

For example, the measurable range is to change x64 to x128, the measured data of x128 is represented as half value compared to that of x64 for the same incident light.

## 7. REGISTER MAP

There are 11 registers in YL-2023F-UVADS(A). Those registers can be accessed through I<sup>2</sup>C interface from host CPU. The register map is shown in table 7.1.

*All the reserved registers are recommended NOT to be read and written and the reserved fields are recommended to be filled with '0'.*

Addr (Hex)	Alias	Bit								Init (Hex)
		7	6	5	4	3	2	1	0	
0x00	CHIPID	CHIPID[7:0]								0x62
0x01	MODE	Reserved	UVA_EN			Reserved	POWER_MODE[1:0]		0x03	
0x02	Reserved	Reserved								
0x03	Reserved	Reserved								
0x04	RES_UV	Reserved				RES_UV[2:0]				0x03
0x05	RANGE_UVA	Reserved				RANGE_UVA[2:0]				0x07
0x06	Reserved	Reserved								
0x07	Reserved	Reserved								
0x08	Reserved	Reserved								
0x09	Reserved	Reserved								
0x0A	MODE_CTL	SLEEP_PERIOD[3:0]				Reserved				
0x0B	SOFT_RESET	SOFT_RESET[7:0]								0x00
0x0C~0x14	Reserved	Reserved								
0x15	UVA_LSB	UVA[7:0]								ReadOnly
0x16	UVA_MSB	UVA[15:8]								ReadOnly
0x17	Reserved	Reserved								
0x18	Reserved	Reserved								
0x30	NVM_Read_ctrl	NVM Read Address[7:0]								
0x31	NVM_MSB	NVM(non-volatile memory)data output [15:8]								ReadOnly
0x32	NVM_LSB	NVM(non-volatile memory)data output [7:0]								ReadOnly

Table 7.1 Register map

### Register 0x00 – CHIPID

D7	D6	D5	D4	D3	D2	D1	D0
CHIPID							

It stores CHIPID. The CHIPID always maintains '0x62'.

### Register 0x01 – MODE

D7	D6	D5	D4	D3	D2	D1	D0
		OPER[1:0]				PMODE[1:0]	

This field controls UVA sensing operation. According to the value, UVA sensing operation can be enabled or disabled.

**Table 7.2 Sensor Operations**

OPER[1 :0]	Operations
00	No operation
01	UVAoperation
10, 11	Not used

### PMODE[1:0]

This field controls the power management modes. Initial state is shutdown mode.

**Table 7.3 Power management modes**

PMODE	Power Management modes
00	Normal mode
01	Low-powermode
10	Auto shutdown mode
11	Shutdown mode

### Register 0x04 – RES\_UV

D7	D6	D5	D4	D3	D2	D1	D0
						RES_UV [2:0]	

### RES\_UV[2:0]

This field defines the measuring period of sensor operation. The default value is '011'.

**Table 7.4Sensor resolution**

RES_UV[2:0]	Resolution	Sensor measuring
000	16bits	800ms
001	16bits	400ms
010	16bits	200ms
<b>011</b>	<b>16bits</b>	<b>100ms</b>
100 ~111	-	Not used

### Register 0x05 – RANGE\_UVA

D7	D6	D5	D4	D3	D2	D1	D0
					RANGE_UVA [2:0]		

### RANGE\_UVA [2:0]

This field defines the range of UVA operation. The default value is '111'.

**Table 7.5UVA range**

RANGE_UVA[2:0]	Measurable
000	x1
001	x2
010	x4
011	x8
100	x16
101	x32
110	x64
<b>111</b>	<b>x128</b>

### Register 0x0A – MODE\_CTL

D7	D6	D5	D4	D3	D2	D1	D0
		SLP_PER[2:0]					

### SLP\_PER[2:0]

This field defines sleep duration in low-power mode. The sleep duration is based on measuring time of each operating mode.

**Table 7.7Sleep duration**

SLP_PER[2:0]	Sleep duration
000	2 times
001	4 times
010	8 times
011	16 times
100	32 times
101	64 times
110	128 times
111	256 times

### Register 0xB – SOFT\_RESET

D7	D6	D5	D4	D3	D2	D1	D0
SOFT_RESET							

### SOFT\_RESET[7:0]

If 0xA5 is written into this register, all the circuits and registers are initialized. Since it is

auto-cleared, it always indicates 0x00 when host CPU reads it out.

It should be noted that applying SOFT\_RESET should be done only when POWER\_MODE='00'.

### Register 0x15 – UVA\_LSB

D7	D6	D5	D4	D3	D2	D1	D0
UVA[7:0]							

#### UVA [7:0]

UVA data lower 8 bits.

### Register 0x16 – UVA\_MSB

D7	D6	D5	D4	D3	D2	D1	D0
UVA[15:8]							

#### UVA[15:8]

UVA data upper 8 bits.

### Register 0x30 – NVM Read Control

D7	D6	D5	D4	D3	D2	D1	D0
NVM address for read							

#### NMVaddress[7:0]

If NVM(non-volatile memory) address is written into this register,NVM gives out the memory content through NVM data output registers (register 0x31, 0x32)

**Table 7.8NVM address for read**

address	NVM READ ADDRESS
0x0A	offset
0x0B	A_Scale

Example) - Offset

```
//Read the value of NVM
ADDRESS0x0A(offset)
```

```
// ***** NVM Read Command***** //
`I2C_WRITE(`DEVADDR, 8'h30, 8'h0A); // NVM
ADDRESS
//As the data size of Offsetis 8bit, Offset data
can be read out through NVM MSB
register(0x31)
Offset = I2C_READ(`DEVADDR, 8'h31); // NVM
DATA MSB [15:8]
// ***** NVM DataRead Command***** //
A_Scale_msb = I2C_READ(`DEVADDR, 8'h31); //
NVM DATA MSB [15:8]
```

Example) – A\_Scale

```
//Read the value of NVM ADDRESS 0x0B(A
Scale)
// ***** NVM Read Command***** //
`I2C_WRITE(`DEVADDR, 8'h30, 8'h0B); // NVM
ADDRESS
```

```
//As the data size of A_Scale is 16bit,so
through I2C need to read for a two times
// ***** NVM DataRead Command***** //
A_Scale_msb = I2C_READ(`DEVADDR, 8'h31); //
NVM DATA MSB [15:8]
A_Scale_lsb = I2C_READ(`DEVADDR, 8'h32); //
NVM DATA LSB [15:8]
```

### Register 0x31 – NVM\_MSB

D7	D6	D5	D4	D3	D2	D1	D0
NVM data[15:8]							

#### NVM data[15:8]

NVM data upper 8 bits.

### Register 0x32 – NVM\_LSB

D7	D6	D5	D4	D3	D2	D1	D0
NVM data[7:0]							

#### NVM data [7:0]

NVM data lower 8 bits.

## 8. I<sup>2</sup>C INTERFACE

I<sup>2</sup>C slave interface is implemented on the basis of "I<sup>2</sup>C Specification UM10204 Rev. 03 (19 June 2007)". The 7-bit device address is "0111001", which can be modified by bonding option.

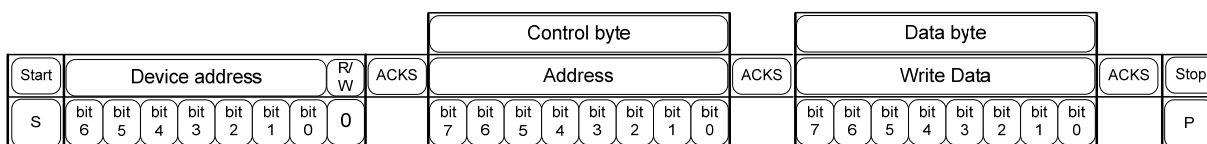
To explain the read/write operations of I<sup>2</sup>C interface, some abbreviations are introduced as follows.

**Table 8.1 Abbreviations**

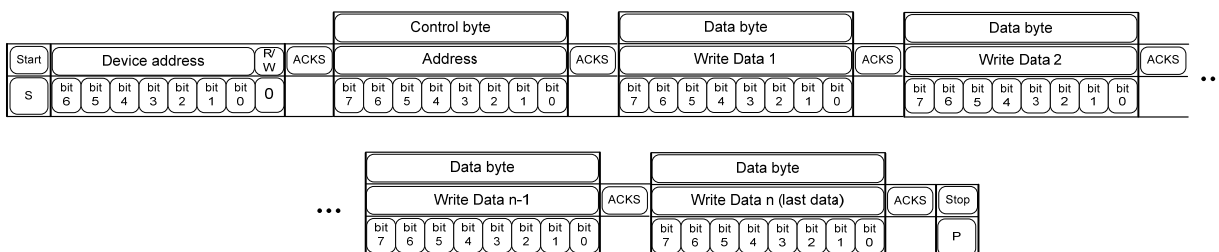
Abbr.	Operation
S	Start condition
Sr	Repeated start condition
P	Stop condition
ACKS	Acknowledged by slave
ACKM	Acknowledged by master
NACKS	Not acknowledged by slave
NACKM	Not acknowledged by master

In write operation, after host CPU sends start signal, first byte contains read/write mode and device address information. MSB 7 bits of first byte express device address and last bit indicates read ('1') or write ('0'). As soon as slave receives data, it needs to respond ACKS or NACKS. If host CPU receives ACKS, it sends the register address to YL-2023F-UVADS(A). Last transfer starts to send register data being written to its address. When the received information is NACKS, host CPU should finish the communication as sending stop condition. Likewise, host CPU sends stop condition after normal operation completion.

I<sup>2</sup>C burst write operation was implemented to send registers continuously. In figure 8.2, the fourth and fifth bytes can be continuously sent to slave without stop condition. The register address increments automatically and I<sup>2</sup>C slave receives data. The burst write does not finish until host CPU sends stop signal.



**Figure 8.1 I<sup>2</sup>C single write operation**



**Figure 8.2 I<sup>2</sup>C burst write operation**

I<sup>2</sup>C read operation consists of two stage. The first communication terminates when host CPU sends stop condition after the first byte transfer for device address setting and the second byte transfer for slave address setting is completed. Secondly, host CPU sends start condition again, device address and read mode '0' as the first byte for read operation. And then I<sup>2</sup>C slave should send register data of the corresponding register address defined in the previous stage. For I<sup>2</sup>C burst read operation, if host CPU sends SCL clock continuously, I<sup>2</sup>C slave must send data in consecutively increasing address order. To terminate the communication, stop condition should be sent to I<sup>2</sup>C slave.

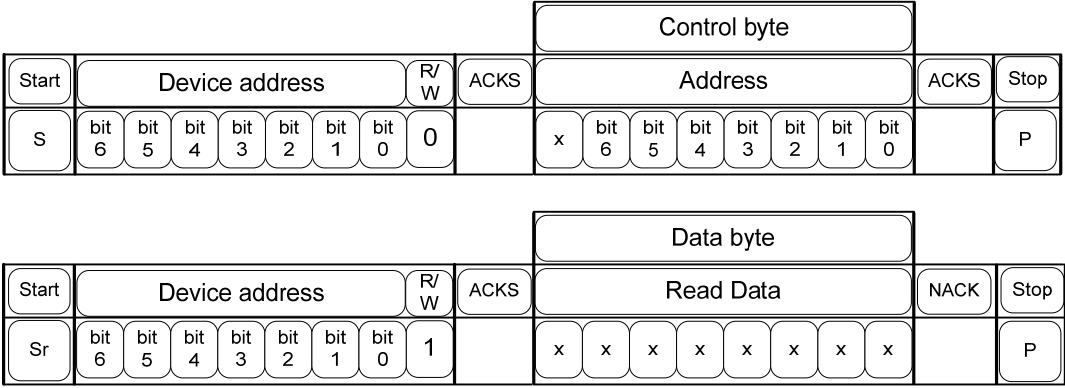


Figure 8.3 I<sup>2</sup>C single read operation

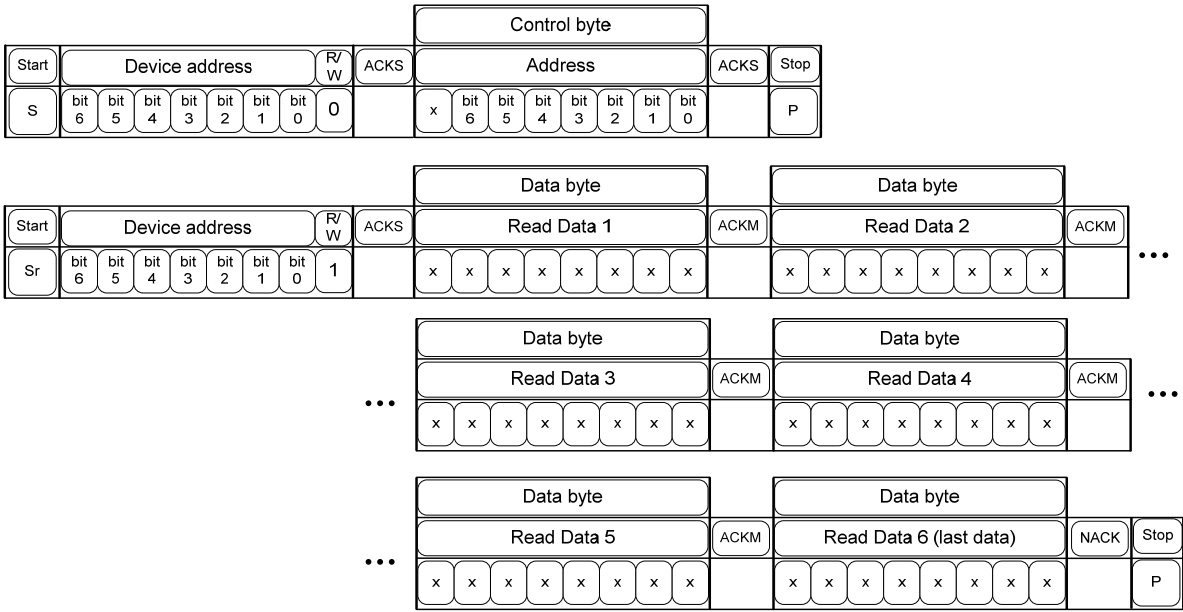
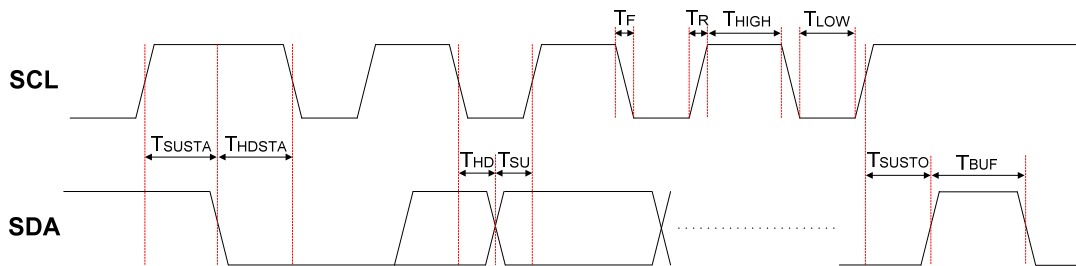


Figure 8.4 I<sup>2</sup>C burst read operation

The timing parameters and timing diagram for I<sup>2</sup>C operations are shown in table 8.2 and figure 8.5 as follows.

**Table 8.2 I<sup>2</sup>C timing parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Units	Test
SCL Freq	SCL frequency				400	KHz	Q
T <sub>F</sub>	Fall time				300	ns	Q
T <sub>R</sub>	Rise time				1000	ns	Q
T <sub>HIGH</sub>	SCL high time		0.6			μs	Q
T <sub>LOW</sub>	SCL low time		1.3			μs	Q
T <sub>SUSTA</sub>	Start condition setup time		0.6			μs	Q
T <sub>HDSTA</sub>	Start condition hold time		0.6			μs	D
T <sub>HD</sub>	Data hold time		0.0			μs	Q
T <sub>SU</sub>	Data setup time		0.1			μs	Q
T <sub>SUSTO</sub>	Stop condition setup time		0.6			μs	Q
T <sub>BUF</sub>	Bus free time		1.3			μs	Q



**Figure 8.5 I<sup>2</sup>C timing diagram**

## 9. TYPICAL CHARACTERISTICS

TBD

**Figure9.1 Output data – UV Intensity Characteristics**

TBD

**Figure9.2 Spectral Responsivity Characteristics**