DESCRIPTION

The PT16750 is a Headlight LED controller for automotive. The controller can support multiple DC-DC topologies, such as Buck, Boost, SEPIC driver topologies. The controller implements a fixed-frequency peak current mode control technique, integrated programmable switching frequency, slope compensation, and soft-start timing. It incorporates a high voltage (65 V) rail-to-rail current sense amplifier, which can directly measure LED current using a high-side series sense resistor. The amplifier is designed to achieve better current accuracy than ±3%, in the junction temperature range of 25°C to 140°C and output common-mode voltage range of 3 to 60 V.

LED current can be modulated using either analog dimming or PWM dimming techniques. Adjust IADJ input voltage from 140 mV to 2.25 V to realize linear analog dimming. PWM dimming of LED current is achieved by modulating the PWM input pin with the desired duty cycle and frequency. DDRV gate driver output can be used to enable series FET dimming functionality to get over 1000:1 contrast ratio.

The PT16750 provides current monitor function, check the LED status continuous through the IMON pin. This allows for LED short circuit or open circuit detection and protection. Additional fault protection features include VCC UVLO, output OVP, switch cycle-by-cycle current limit, and thermal protection.

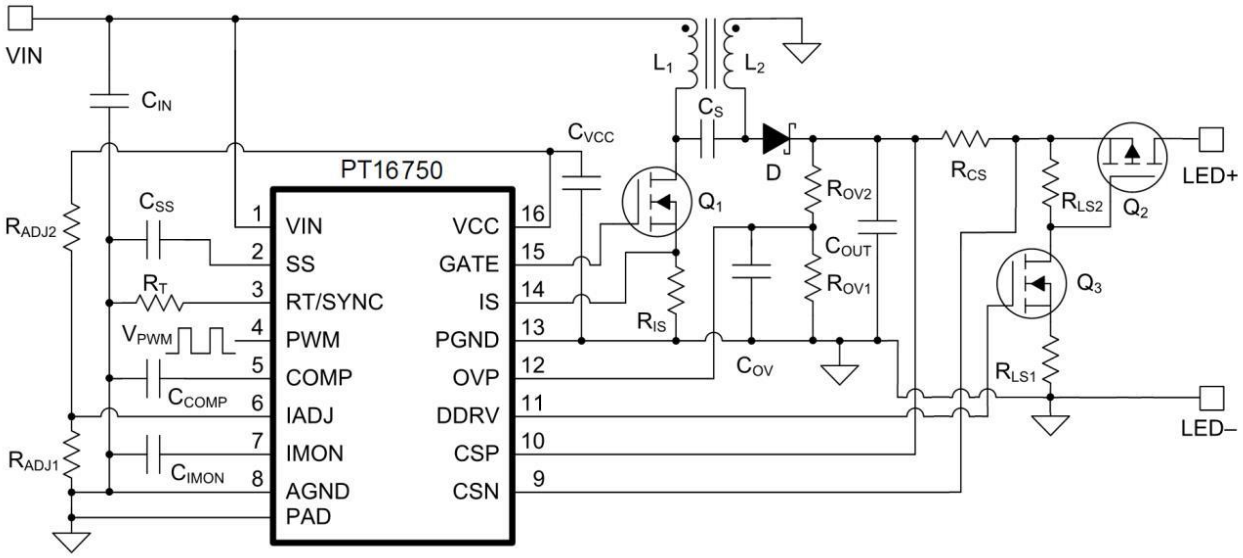
FEATURES

- Automotive AEC-Q100, Grade 1 (-40℃~+125℃) Qualified.
- Input Voltage: 4.5V-65V
- Output Voltage: 3V to 65V
- LED Current Accuracy: ±3%
- High-Side Current Sense Implementations
- Analog LED Current Adjust (IADJ) With over 15:1 Contrast Ratio
- Integrated Series N-Channel dimming driver Interface, supports over 1000:1 Series FET PWM Dimming Ratio
- Programmable Switching Frequency With External Clock Synchronization Capability
- Programmable Soft-Start and Slope Compensation
- Continuous LED Current Monitor Output for System Fault Detection and Diagnoses
- Comprehensive Fault Protection Circuitry Including VCC Undervoltage Lockout (UVLO), Output Overvoltage Protection (OVP), Cycle-by-Cycle Switch Current Limit, and Thermal Protection

APPLICATIONS

- Automotive Headlight LED Drive
- High-Brightness LED Applications
- Exit Signs and Emergency Lighting

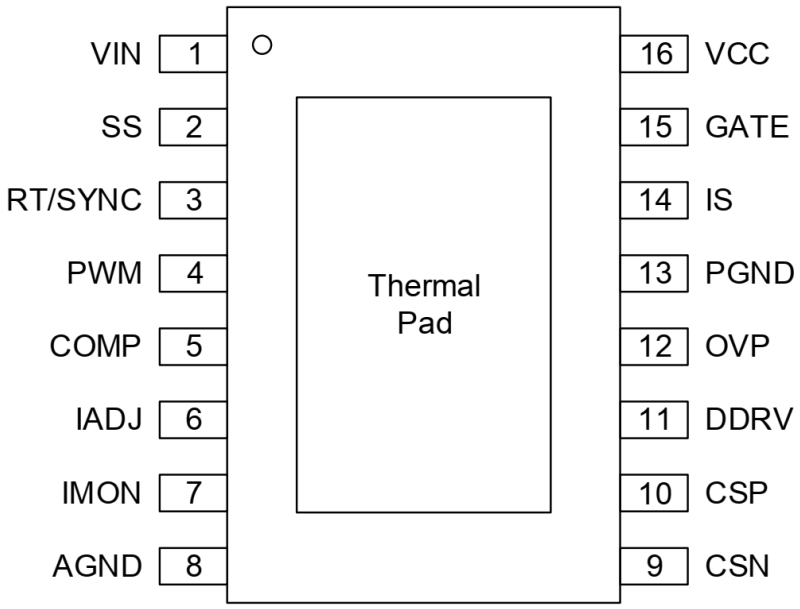
TYPICAL APPLICATION



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16750-HT	HTSSOP 16pins	PT16750-HT

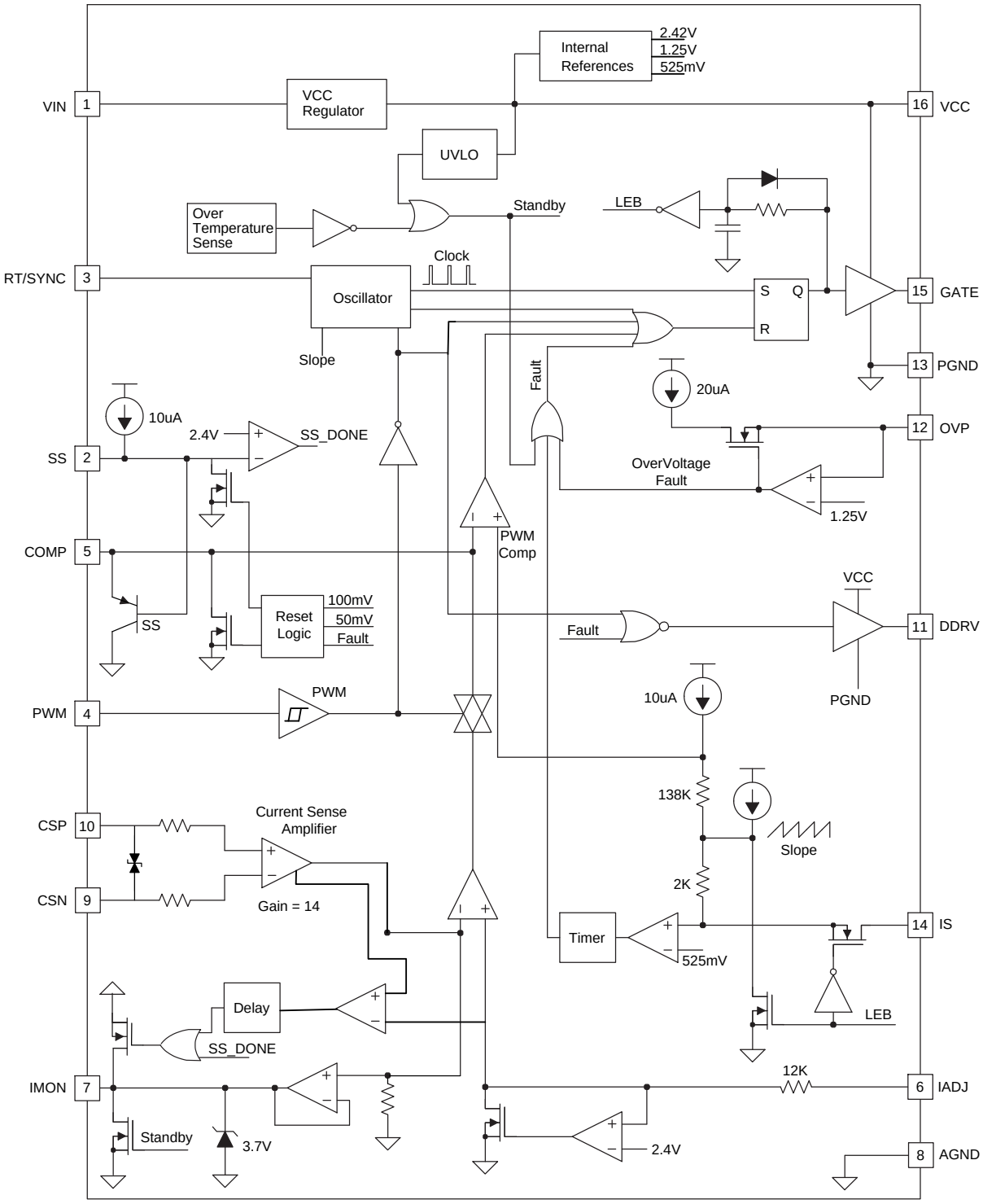
PIN CONFIGURATION



PIN DESCRIPTION

PIN Name	I/O	Description	Pin No.
VIN	--	Supply voltage input. Place a 100nF capacitor close to the controller.	1
SS	I/O	Programmable soft-start pin. Connect a capacitor to AGND to set the start-up time. Short this pin to AGND to disable the Gate pin work.	2
RT/SYNC	I/O	Programmable oscillator frequency pin. Connect a resistor to AGND to set the switching frequency. Connect a 100nF capacitor series to this pin to synchronize the internal oscillator from an external clock pulse.	3
PWM	I	PWM dimming input. In the PWM dimming mode, the input signal duty cycle controls the LED average current. Connect PWM pin to VCC when not used for PWM dimming. Pull this pin below 2.3 V to turn off switching, and set DDRV output to ground.	4
COMP	I/O	Error amplifier compensation. Connect compensation network to achieve desired closed loop response.	5
IADJ	I	Reference voltage input for LED current. To implement analog dimming, source a external voltage from 0V to 2.25V to this pin, and the current sense voltage: $V_{(CSP-CSN)} = V_{IADJ}/14$. Connecting IADJ to VCC with 100kΩ series resistor, the reference voltage would be clamped to 2.42 V and the current sense threshold, $V_{(CSP-CSN)}$ = 172 mV.	6
IMON	O	LED current status report pin. The pin reports LED current as $V_{IMON} = 14 \times I_{LED} \times R_{CS}$. Bypass with a 1nF ceramic capacitor to AGND.	7
AGND	--	Analog ground. Return for the internal voltage reference and analog circuit.	8
CSN	I	Current sense amplifier negative input (–). Connect directly to the negative node of LED current sense resistor R_{CS}.	9
CSP	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor R_{CS}.	10
DDRV	O	Gate driver output for series dimming MOSFET. Connect to a level-shift circuit with P-channel MOSFET to implement series FET PWM dimming.	11
OVP	I	Overvoltage protection pin. Connect resistor divider from output to set overvoltage protection threshold and hysteresis.	12
PGND	--	Power ground. Return for GATE and DDRV drivers. Connect to circuit ground, GND, to complete return path.	13
IS	I	Switching current sense pin. Connected to switching current sense resistor, R_{IS}, to monitor the peak current of the main MOSFET.	14
GATE	O	Gate driver output for switching MOSFET. Connect to gate of the main MOSFET.	15
VCC	--	VCC bias supply pin. Using a 2.2μF to 4.7μF ceramic capacitor located close to the controller.	16
Thermal PAD	--	Thermal pad. This PAD must be connected to PCB ground plane using multiple vias for good thermal performance.	Thermal PAD

FUNCTIONAL BLOCK DIAGRAM



FUNCTION DESCRIPTION

OPERATION

The PT16750 is a wide input range (4.5 V to 65 V) LED driver controller. It has all of the functions necessary to implement a compact and highly efficient LED driver, supports step-up or step-down converter topologies. It incorporates a low input offset, rail-to-rail current sense amplifier that supports a wide range of output voltages (3 V to 65 V) and is capable of powering the LED string consisting of 1 to more than 20 LEDs. The device works at fixed-frequency, peak current mode control, provides high-side current shunt sensing technique to achieve a constant current output, and drive a single string of series-connected LEDs. The LED current sense threshold, set by the analog adjust input, IADJ, provides the capability to analog (amplitude) dim over a linear range of 15:1 by varying the voltage, V_{IADJ}, from 140 mV to 2.25 V. The IADJ input provides a way to externally program LED current and facilitates calibration, brightness correction, and thermal management of the LEDs. High resolution and linear dimming response is achieved by varying the duty cycle of LED current based on the PWM input. When using an external P-channel MOSFET in series with the LED load, the PWM input directly controls the GATE and DDRV drive outputs, controls the internal oscillator, and enables high-speed PWM dimming with a contrast of over 1000:1. The current monitor output, IMON, reports the instantaneous status of LED current measured by the rail-to-rail current sense amplifier. This function is incorporated to indicate LED short and open circuit failures and enables cable harness fault detection independent of LED driver topology. Other fault protection functions include cycle-by-cycle current limiting, overvoltage protection with hysteresis, VCC undervoltage protection, thermal shutdown, and remote shutdown through pulling down the SS pin.

OSCILLATOR

The switching frequency of PT16750 can be programmed by a single external resistor connected between the RT/SYNC pin and the AGND pin. To set a desired frequency, f_{SW} (Hz), the resistor value can be calculated using:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{sw})^{1.047}} \ (\Omega)$$

Figure 1 shows a curve of switching frequency versus resistance, RT. It suggests that the switching frequency should be set between 80 kHz and 700 kHz in order to obtain optimal performance and best efficiency in the range of input and output voltage. Working at higher switching frequencies requires careful selection of N-channel MOSFET characteristics. Additional switching losses and junction temperature rise should be considered.

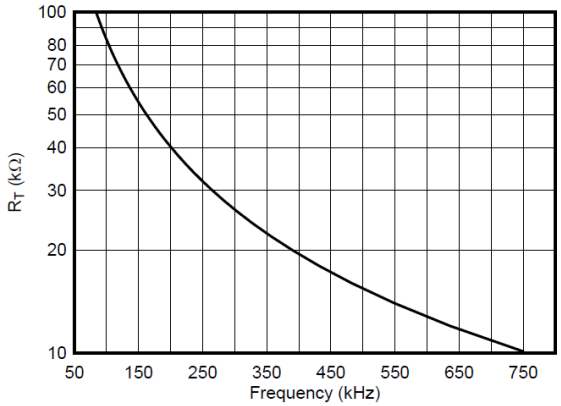


Figure 1. RT vs Switching Frequency

The internal oscillator can be synchronized by AC-coupled external clock pulse to RT/SYNC pin, shown as in Figure 2. The positive going synchronization clock at the RT pin must exceed the RT/SYNC threshold, and the negative going synchronization clock at the RT pin must exceed the RT/SYNC falling threshold so that the internal synchronization pulse detector can be tripped.

It recommends that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the RT resistor. A minimum coupling capacitor of 100 nF and typical pulse width of 100 ns for proper synchronization are recommended. In the case where external synchronization clock is lost the internal oscillator takes control of the switching rate based on the RT resistor to maintain output current regulation. The RT resistor is always required whether the oscillator is free running or externally synchronized.

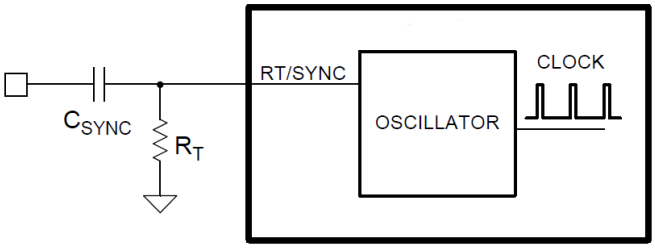


Figure 2. Oscillator Synchronization through AC Coupling

RAIL-TO-RAIL CURRENT SENSE AMPLIFIER

The PT16750 incorporates a high voltage rail-to-rail current sense amplifier to measure the average current of LED string based on the differential voltage drop between the CSP and CSN inputs over a common mode range of 3 V to 65 V. The differential voltage, V_{CSP}-V_{CSN} is amplified by a voltage-gain factor of 14, and connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage, (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) to less than 5 mV over the recommended common-mode voltage, and temperature range.

Figure 3 shows a recommended common-mode or differential mode low-pass filter circuit, which can be used to eliminate the effects of large output current ripple and switching current spikes caused by diode reverse recovery. PT16750 recommends that the filter resistance should be between 10 Ω and 100 Ω to limit the additional offset caused by amplifier bias current and achieve best accuracy and line regulation.

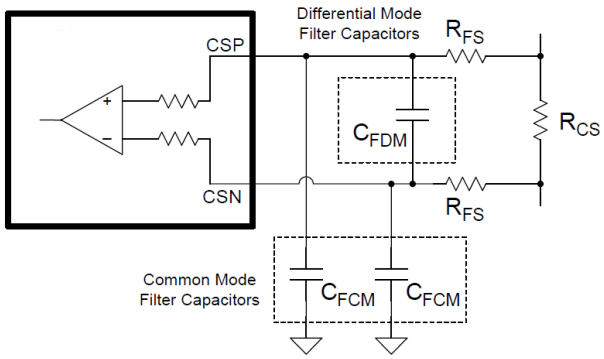


Figure 3. Current Sense Amplifier Input Filter Options

GATE DRIVER

The PT16750 contains an N-channel gate driver for switching output V_{GATE} between VCC and PGND. The peak source and sink current of 500 mA allows slew-rate control of the MOSFET gate and drain node voltages, limits the Conducted Emission and Radiation Emission generated by switching. The gate driver supply current $I_{CC(GATE)}$ depends on the total gate drive charge (Q_G) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{CC(GATE)}=Q_G \times f_{SW}$. PT16750 recommends to choose a low gate charge specification MOSFET to limit the junction temperature rise and switch transition losses.

While choosing the N-channel MOSFET device, consider the threshold voltage when operating in the dropout region when V_{IN} is below the V_{CC} regulation level. It recommends a logic level device with a threshold voltage below 5 V when the device is required to operate at an input voltage less than 7 V.

SWITCH CURRENT SENSE AND INTERNAL SLOPE COMPENSATION

PT16750 is a peak current mode controller, monitors the main MOSFET current by IS pin. The duty cycle of GATE output is derived by comparing the peak switching current which measured by the R_{IS} resistor, to the internal COMP voltage threshold. An internal slope signal is added to the measured sense voltage, V_{IS}, to prevent subharmonic oscillations for duty cycles greater than 50%. The linear slope voltage, V_{SL}, of fixed amplitude 200 mV, is derived from a 100-µA sawtooth ramp current synchronized to the internal oscillator frequency. An internal blanking circuit prevents MOSFET switching current spike propagation and premature termination of duty cycle by internally shunting the IS input for 150 ns after the beginning of the new switching period. It recommends using an external low-pass RC filter with resistor values ranging from 100 Ω to 500 Ω to provide additional noise suppression when operating in the dropout region (VIN less than 7 V).

Cycle-by-cycle current limit is accomplished by a redundant internal comparator, which immediately terminates the GATE output when the IS input voltage, V_{IS}, exceeds 525 mV (typ) threshold. When a current limit occurs, the SS and COMP pin are internally grounded to reset the state of the controller. The GATE output is enabled after the expiration of the 35 µs internal fault timer and a new start-up sequence is initiated through the SS pin.

TRANSCONDUCTANCE ERROR AMPLIFIER

The internal transconductance amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and the external IADJ input voltage. Closed-loop regulation is achieved by connecting a compensation network to the output of the error amplifier. In most LED driver applications, a simple integral compensator consists of a capacitor across the COMP output and ground, to obtain a stable response. It recommends a capacitor value between 10 nF and 100 nF as a good starting point. Higher closed-loop bandwidth can be achieved by implementing a proportional-integral compensator consisting of a series resistor and a capacitor network connected across the COMP output and ground. Based on the converter topology, the compensation network should be tuned to achieve a minimum of 60° of phase margin and 10 dB of gain margin.

SOFT-START

The PT16750 has soft-start function to help the regulator reach the steady-state operating point gradually, thus reducing startup stresses and surges. The COMP pin is clamped to the SS pin, separated by a diode, until LED current nears the regulation threshold. The voltage of SS pin increase gradually due to the internal 10-μA soft-start current source on an external soft-start capacitor C_{SS}. This results in a gradual rise of the COMP voltage from GND.
When VCC exceeds the UVLO threshold, the internal 10-μA current source turns on. At the beginning of the soft-start sequence, the SS pull down switch is active and is released when the voltage VSS drops below 25 mV. The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin should be controlled by choosing a compensation capacitor that avoids large startup transients. The value of CSS should be large enough to charge the output capacitor during the soft-start transition period.

ANALOG ADJUST INPUT

The voltage of LED current sense resistor V_{CSP}–V_{CSN}, is regulated to the analog adjust input voltage V_{IADJ}, scaled by the current sense amplifier voltage gain of 14. Using a resistor divider from VREF or a voltage source, the LED current can be linearly adjusted by varying the voltage on IADJ pin from 140 mV to 2.25 V. The IADJ pin can be connected to VREF through an external resistor to set LED current based on internal reference voltage 2.42V. This device provides different methods to set the IADJ voltage. Figure 5 shows how the IADJ input can be used in conjunction with a NTC resistor to achieve the thermal protection. A PWM signal combined with first- or second-order low-pass filter can be used to program the IADJ voltage as shown in Figure 6.

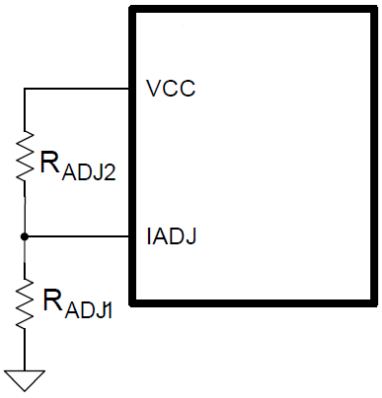


Figure 4. Static Reference Setting Resistor Divider From VCC

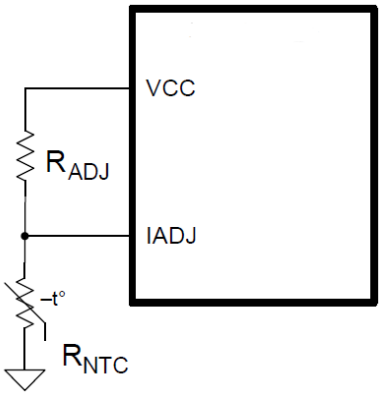


Figure 5. Using External NTC Resistor for Thermal Protection

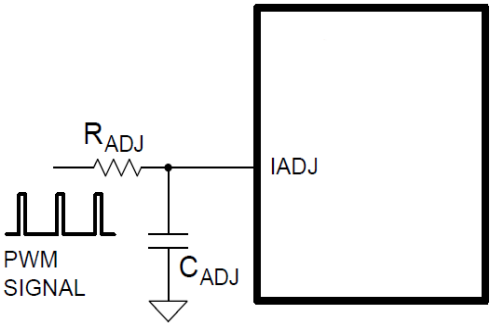


Figure 6. Analog Dimming Achieved By Low-pass Filtering External PWM Signal

PWM INPUT

The PT16750 contains a PWM input for pulse-width modulating, varying the LED brightness. The LEDs' brightness can be linearly varied by modulating the duty cycle of the pulsating voltage source connected to the PWM input pin. When the PWM input below 2.3 V, turns off GATE driving, stops the oscillator, disconnects the COMP pin, and sets the DDRV output to GND in order to maintain the charge on the compensation network and output capacitors. When the PWM input over 2.5V, the GATE and DDRV outputs are enabled to ramp the inductor current to the previous steady-state value. Only when the switch current sense voltage V_{IS} exceeds the COMP voltage(V_{COMP}), the COMP pin is connected and the error amplifier and oscillator are enabled, thus forcing the converter into steady-state operation with minimum LED current overshoot immediately. The PWM pin should be connected to the V_{CC} if dimming is not required. If the PWM input is disconnected or left floating, an internal pull-down resistor sets the input to logic-low and disable the controller working.

VCC REGULATOR AND UNDERVOLTAGE LOCKOUT

The PT16750 integrates a 65V linear regulator to generate 7.5V bias supply (VCC pin) and other internal reference voltages. The VCC pin is monitored to implement UVLO protection. The controller is enabled when the VCC voltage exceeds 4.2V threshold and is disabled when the voltage drops below 4V threshold. The UVLO comparator provides 0.2V hysteresis to avoid chatter during transitions. The UVLO thresholds are fixed internally and cannot be adjusted. The VCC pin provides minimum 36mA supply current (I_{VCC}) for external devices. The VCC supply powers the internal circuitry, GATE driver and DDRV driver. Place a bypass capacitor in the range of 2.2 µF to 4.7 µF across the VCC output and PGND to ensure proper operation. The regulator operates in dropout when input voltage VIN falls below 7.5 V forcing VCC to be lower than VIN by 300 mV for a 20-mA supply current. The VCC is a regulated output of the internal regulator and cannot be driven from an external power supply.

SERIES DIMMING FET GATE DRIVER OUTPUT

The DDRV output can be translated with an external level-shift circuit to drive a high-side series P-channel dimming FET as shown in Figure 7. The series dimming FET is required to achieve high contrast ratio as it ensures fast rise and fall times of the LED current in response to the PWM input.
The series P-channel MOSFETs can also limit the output current when the LED+ is shorted to LED-. Do not leave the DDRV pin unconnected, and the series P-channel MOSFET is necessary.

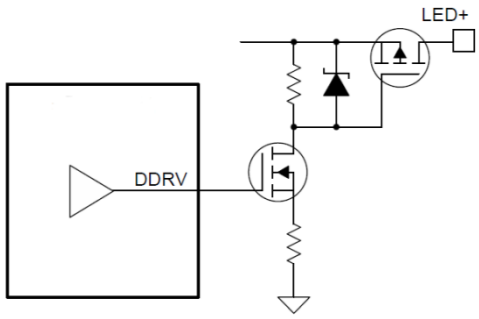


Figure 7. Series Dimming FET Connections

CURRENT MONITOR OUTPUT

The IMON pin voltage represents the LED current measured by the differential voltage drop between the CSP and CSN inputs. The linear relationship between the IMON voltage and LED current includes the amplifier gain-factor of 14 (see Figure 8). The IMON output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection and mitigation based on programmable threshold V_{OCTH}. The IMON voltage is clamped to 3.7V internally.

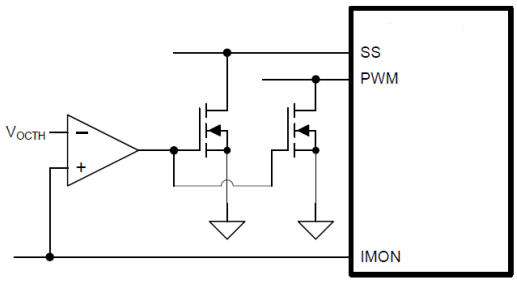


Figure 8. LED Over current Protection using IMON Output

OVERVOLTAGE PROTECTION

The PT16750 includes a dedicated OVP pin which can be used for input or output overvoltage protection. This pin has a precision 1.25V threshold with 20μA of hysteresis current. The overvoltage threshold limit is set by a resistor divider network from the input or output terminal to GND. When the OVP pin voltage exceeds the 1.25V threshold, the GATE and DDRV pins are immediately pulled low and the SS and COMP capacitors are discharged. The GATE is enabled and a new startup sequence is initiated after the voltage of OVP pin drops below the hysteresis threshold set by the 20μA source current and the external resistor divider.

THERMAL PROTECTION

The internal thermal shutdown circuitry is implemented to protect the device when the maximum junction temperature is exceeded. When activated, typically at 175°C, the controller is forced into a shutdown mode, the internal regulator is disabled. This function is designed to prevent the device overheating and even damage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Voltage		VIN, CSP, CSN	-0.3	65	V
		IADJ, IS, PWM, RT/SYNC	-0.3	8.5	V
		OVP, SS	-0.3	5.5	V
		CSP to CSN, PGND	-0.3	0.3	V
Output Voltage		VCC, GATE, DDRV	-0.3	8.5	V
		COMP	-0.3	5.0	V
Source Current		IMON	-	100	µA
		GATE, DDRV (Pulsed <20 ns)	-	500	mA
Sink Current		GATE, DDRV (Pulsed <20 ns)	-	500	mA
Operating Junction Temperature	T_J		-40	150	°C
Storage Temperature	T_{stg}			150	°C

ESD RATINGS

Parameter		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM)	±2000	V
	Charged-device model (CDM)	±800	
	Machine model (MM)	±250	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Input Voltage	VIN	6.5	14	65	V
Current Sense Common Mode	V_{CSP}, V_{CSN}	3		60	V
Switching Frequency	f_{SW}	80		700	KHz
SYNC Frequency	f_{SYNC}	0.8 × f_{sw}		1.2 × f_{SW}	KHz
Current Reference Voltage	V_{IADJ}	0.14		2.42	V
Operating Ambient Temperature	T_A	-40		125	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage (VIN)						
LDO Dropout Voltage	V_{DO}	I_{CC} = 20 mA, V_{IN} = 5V		300		mV
Bias Supply (VCC)						
Regulation Voltage	$V_{CC(REG)}$	No load	7.0	7.5	8.0	V
Supply Undervoltage Protection	$V_{CC(UVLO)}$	VCC rising threshold, V_{IN} = 8V		4.2	4.4	V
		VCC falling threshold, V_{IN} = 8V	3.6	4.0		V
		Hysteresis		200		mV
Supply Current Limit	$I_{CC(LIMIT)}$	V_{CC} = 0V	36	43	46	mV
Supply Stand-by Current	$I_{CC(STBY)}$	V_{PWM} = 0V		1.9	2.1	mV
Supply Switching Current	$I_{CC(SW)}$	V_{CC} = 7.5V, C_{GATE} = 1 nF		6.0	6.6	mV
Oscillator (RT/SYNC)						
Switching Frequency	f_{SW}	R_T = 40 KΩ	180	200	220	KHz
		R_T = 20 KΩ	360	400	440	
RT Output Voltage	V_{RT}			1		V
SYNC Rising Threshold	V_{SYNC}	$V_{RT/SYNC}$ rising		2.7	3.1	V
SYNC Falling Threshold		$V_{RT/SYNC}$ falling	1.8	2		V
Minimum SYNC Clock Pulse Width	$t_{SYNC(MIN)}$			100		ns
Gate Driver (GATE)						
Gate Driver High Side Resistance	R_{GH}	I_{GATE} = –10 mA		6.3		Ω
Gate Driver Low Side Resistance	R_{GL}	I_{GATE} = 10 mA		5.5		Ω
Current Sense (IS)						
Current Limit Threshold	$V_{IS(LIMIT)}$		490	525	550	mV
Leading Edge Blanking Time	$t_{IS(BLANK)}$		100	140	180	ns
Current Limit Fault Time	$t_{IS(FAULT)}$			35		µs
IS to GATE Propagation Delay	$t_{ILMT(DLY)}$	V_{IS} pulsed from 0 to 1 V		100		ns
PWM Comparator And Slope Compensation						
Maximum Duty Cycle	D_{MAX}		90%	93%	94%	
IS to COMP Level Shift Voltage	V_{LV}	No slope compensation added	1.2	1.5	1.8	V
Slope Compensation	V_{SL}	D = D_{MAX} (with max slope compensation)		200		mV
IS Level Shift Bias Current	I_{LV}	No slope compensation added		25		µA
IS Level Shift Source Current	I_{LV} + I_{SL}	D = D_{MAX} (with max slope compensation)		115		µA
Current Sense Amplifier (CSP, CSN)						
Current Sense Unity Gain Bandwidth	$C_{S(BW)}$			500		KHz
CSP, CSN Bias Current	$I_{CS(BIAS)}$	$V_{CSP, CSN}$ = 60 V		4		µA
Current Monitor (IMON)						
IMON Output Voltage Clamp	$V_{IMON(CLP)}$		3.2	3.7	4.2	V
IMON Buffer Offset Voltage	$V_{IMON(OS)}$		-11.4	–1.6	7.3	mV
Analog Adjust (IADJ)						
IADJ Internal Clamp Voltage	$V_{IADJ(CLP)}$	I_{IADJ} = 1µA		2.42		V
IADJ Input Bias Current	$I_{IADJ(BIAS)}$	V_{IADJ} < 2.2V			100	µA
IADJ Current Limiting Series Resistor	$R_{IADJ(LMT)}$	V_{IADJ} > 2.6V		12		KΩ
Error Amplifier (COMP)						
Transconductance	gM			120		µA/V
COMP Current Source Capacity	$I_{COMP(SRC)}$	V_{IADJ} = 1.4 V, $V_{(CSP-CSN)}$ = 0 V		132		µA
COMP Current Sink Capacity	$I_{COMP(SINK)}$	V_{IADJ} = 0 V, $V_{(CSP-CSN)}$ = 0.1 V		135		µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier Bandwidth	$EA_{(BW)}$	–3 dB		5.2		MHz
COMP Pin Reset Voltage	$V_{COMP(RST)}$			100		mV
COMP Discharge FET Resistance	$R_{COMP(DCH)}$			240		Ω
Soft-Start (SS)						
Soft-Start Source Current	I_{SS}		7	10	13	µA
Soft-Start Pin Reset Voltage	$V_{SS(RST)}$			25		mV
SS Discharge FET Resistance	$R_{SS(DCH)}$			250		Ω
Overvoltage Protection (OVP)						
OVP Detection Threshold	$V_{OVP(THR)}$		1.18	1.25	1.31	V
OVP Hysteresis Current	$I_{OVP(HYS)}$			20		µA
PWM Input (PWM)						
Schmitt Trigger Logic Level (High Threshold)	$V_{PWM(HIGH)}$			2.5		V
Schmitt Trigger Logic Level (Low Threshold)	$V_{PWM(LOW)}$			2.3		V
PWM Pull Down Resistance	$R_{PWM(PD)}$			1		MΩ
PWM to DDRV Rising Delay	$t_{DLY(RISE)}$			50		ns
PWM to DDRV Falling Delay	$t_{DLY(FALL)}$			70		ns
PWM Gate Drive Output (DDRV)						
DDRV High-Side Resistance	R_{DH}			6.0		Ω
DDRV Low-Side Resistance	R_{DL}			5.0		Ω
Thermal Shutdown						
Thermal Shutdown Temperature				175		°C
Thermal Shutdown Hysteresis				30		°C

DESIGN GUIDE

APPLICATION CIRCUIT

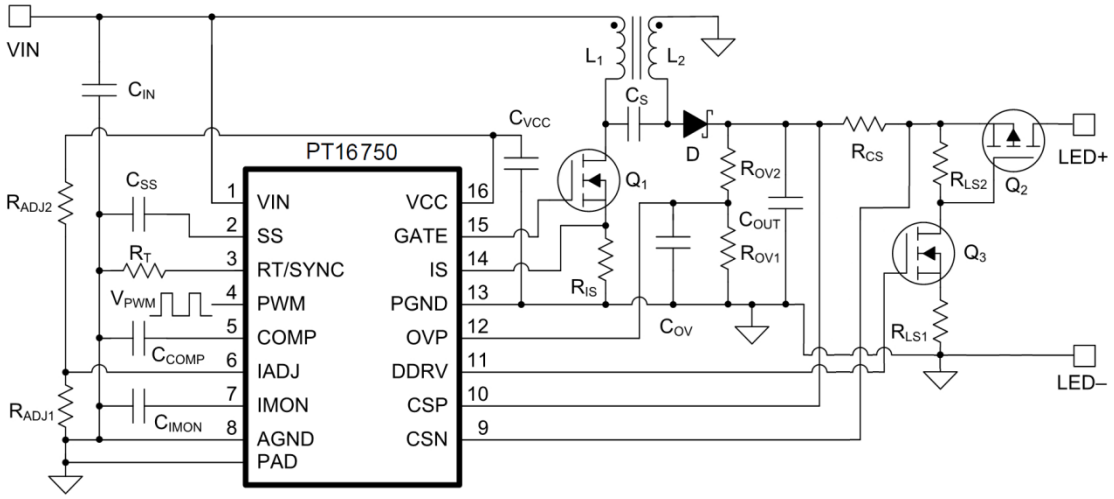


Figure 9. SEPIC LED Driver

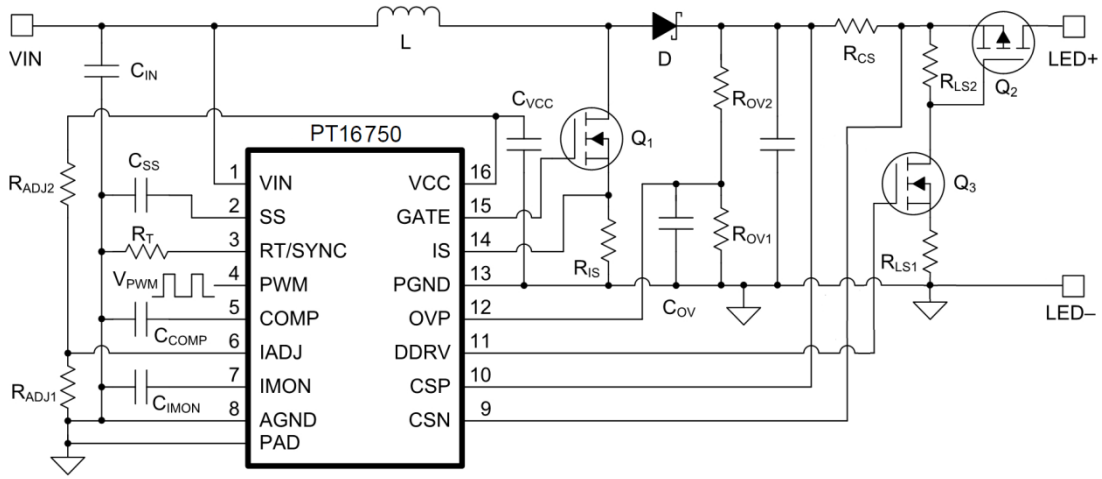


Figure 10. Boost LED Driver

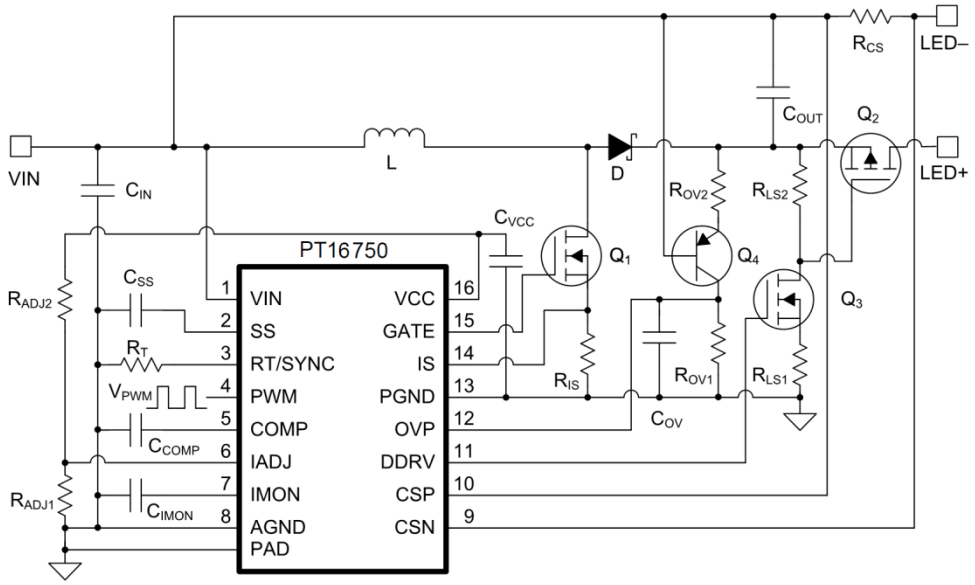


Figure 11. Buck-Boost LED Driver

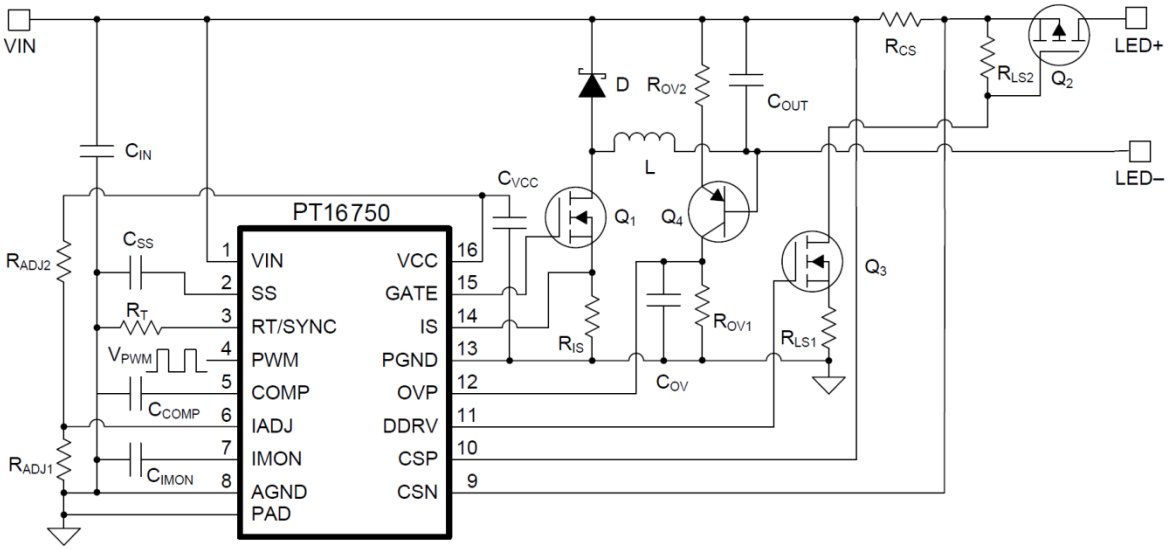


Figure 12. Buck LED Driver

DESIGN PROCEDURE

1. Duty Cycle Calculation

The switching duty cycle (D) defines the converter operation, and is related to the input and output voltages. In steady state, the duty cycle is calculated using following expression:

Buck:	Boost:	SEPIC/Buck-Boost:
$D = \frac{V_O}{V_{IN}}$	$D = \frac{V_O - V_{IN}}{V_O}$	$D = \frac{V_O}{V_O + V_{IN}}$
$D_{MIN} = \frac{V_O}{V_{IN(MAX)}}$	$D_{MIN} = \frac{V_O - V_{IN(MAX)}}{V_O}$	$D_{MIN} = \frac{V_O}{V_O + V_{IN(MAX)}}$
$D_{MAX} = \frac{V_O}{V_{IN(MIN)}}$	$D_{MAX} = \frac{V_O - V_{IN(MIN)}}{V_O}$	$D_{MAX} = \frac{V_O}{V_O + V_{IN(MIN)}}$

The duty cycle must be within the operating range of the controller to ensure that the closed-loop LED current regulation is in the specified input and output voltage range.

2. Inductance Calculation

Consider a good compromise between core loss and copper loss of the inductor, the inductor peak-to-peak ripple current, $\triangle i_{L\text{-}PP}$, is typically set between 20% and 80% of the maximum inductor current, I_L. Higher ripple inductor current allows a smaller inductor size, but needs more capacitors on the output to smooth the LED current ripple. Knowing the desired ripple ratio RR, switching frequency f_{SW}, maximum duty cycle D_{MAX}, and the typical LED current I_{LED}, the inductor value can be calculated as follows:

Buck:

$$\Delta i_{L(PP)} = RR \times I_L = RR \times I_{LED}$$

$$L = \frac{(V_{IN(MIN)} - V_O) \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

Boost and Buck-Boost (SEPIC):

$$\Delta i_{L(PP)} = RR \times I_L = RR \times \frac{I_{LED}}{1 - D_{MAX}}$$

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

As an alternative, the inductor can be selected based on CCM-DCM boundary condition specified based on output power, $P_{O(BDRY)}$. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated based on the lowest LED current and the lowest output voltage requirements for a given application.

$$P_{O(BDRY)} \leqslant I_{LED(MIN)} \text{ X } V_{O(MIN)}$$

Buck:

$$L = \frac{V_{O(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{OUT(MAX)}}{V_{IN}})$$

Boost:

$$L = \frac{V_{IN}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{IN}}{V_{O(MAX)}})$$

Buck-Boost and SEPIC:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times (\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN}})^2}$$

Select inductor with saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

$$I_{L(PK)} = I_L + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}}$$

3. Input Capacitor Value Calculation

The input capacitors (C_{IN}) smooth the input voltage ripple and store energy to supply input current during input voltage drop or PWM dimming transients. In the Boost, SEPIC, and Cuk topology, the series inductor provides continuous input current so smaller input capacitors are required to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$.

The Buck and Buck-Boost topology have discontinuous input current, and larger capacitors are required to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

Buck:

$$C_{IN} = \frac{I_{LED} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta v_{IN(PP)}}$$

Boost:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}}$$

Buck-Boost:

$$C_{IN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta v_{IN(PP)}}$$

For most applications, it highly recommends to select X7R dielectric-based ceramic capacitors due to their low ESR, high ripple current rating, and good temperature performance. For PWM dimming application, aluminum electrolytic capacitor and ceramic capacitor are recommended to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

Decouple VIN pin with a 0.1-μF ceramic capacitor, placed as close as possible to the device and a series 10Ω resistor to create a 150-kHz low-pass filter and eliminate undesired high-frequency noise.

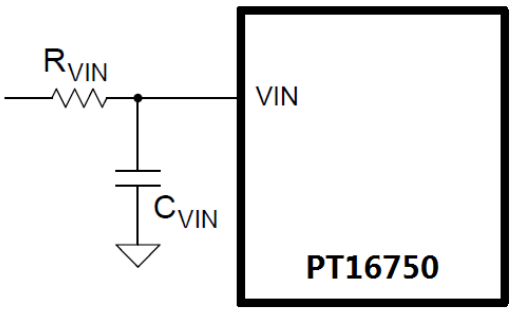


Figure 13. VIN Filter

4. Output Capacitor Value Calculation

Using the output capacitors to attenuate the discontinuous or large ripple current generated by switching and achieve the desired LED output current ripple, $\triangle i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current can be calculated based on following equations.

Buck:

$$C_{OUT} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

Boost and Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

For the Buck topology, the inductor is in series with LED load and requires a smaller capacitor than the Boost, Buck-Boost, and SEPIC topologies to achieve the same LED ripple current.

The ESR and the ESL characteristics must be considered when selecting the output capacitors, as they directly impact the LED current ripple. Ceramic capacitors are the best choice because of its low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions.

It is recommended to use X7R dielectric with rated voltage greater than the maximum LED voltage. Aluminum electrolytic capacitors can be used in parallel with ceramic capacitors to provide large capacity energy storage. The aluminum capacitors must have the necessary RMS current and temperature ratings to ensure extended operating lifetime. The minimum allowable output capacitor RMS current rating, $I_{COUT(RMS)}$, can be approximated:

Buck:

$$I_{COUT(RMS)} = \frac{\Delta i_{LED(PP)}}{\sqrt{12}}$$

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

For applications that need to support different LED string configurations with a wide range of programmable LED current set points, rearrange the previous expressions based on the maximum output power to reflect output capacitance, to ensure that LED current ripple meets the requirements over the entire range of operation.

5. LED Current Programming

The LED current is set by the current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The current sense resistor is placed in series with the LED load. The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the RCS resistor to achieve closed-loop regulation. When VIADJ > 2.42 V, the internal reference clamps the $V_{(CSP-CSN)}$ to 0.173V, the LED current is set by flowing equation :

$$I_{LED} = \frac{0.173}{R_{CS}}$$

The LED current can be programmed by varying V_{IADJ} between 140 mV to 2.25 V. The LED current can be calculated using:

$$I_{LED} = \frac{V_{IADJ}}{14 \times R_{CS}}$$

Using a low-pass common-mode filter consisting of 10Ω resistors in series with CSP and CSN inputs, and place 0.01uF capacitor to ground to the minimize the impact of voltage ripple and noise on LED current accuracy (see Figure 3).

A 0.1μF capacitor across CSP and CSN is included to filter high-frequency differential noise.

6. PWM Dimming Suggestion

Using a MOSFET in series with high-side LED output for PWM dimming. The DDRV output can be translated with an external level-shift circuit to drive the P-channel MOSFET. This MOSFET should have a voltage rating greater than the output voltage, V_O, and a current rating at least 10% higher than the nominal LED current, I_{LED}.
It is important to consider the FET input capacitance and on-resistance as it impacts the accuracy and efficiency of the LED driver. It recommends a FET with lower input capacitance and gate charge to minimize the errors caused by rise and fall times when PWM dimming at low duty cycles. When a high-side P-channel dimming MOSFET is used, the rise and fall times can be controlled by selecting appropriate resistors for the level-shift network, RLS1 and RLS2, as shown in Figure 9 to Figure 12.

7. Main Power MOSFET Selection

The power MOSFET should be able to endure the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. In order to ensure safe operation, the drain voltage VDS is at least 20% greater than the maximum switch node voltage. The MOSFET Drain-Source breakdown voltage, V_{DS}, and RMS current ratings are calculated using the following expressions.
Buck:

$$V_{DS} = V_{IN(MAX)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \sqrt{D_{MAX}}$$

Boost:

$$V_{DS} = V_{O(OV)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Buck-Boost:

$$V_{DS} = (V_{IN(MAX)} + V_{O(OV)}) \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Where the voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions.

A MOSFET with low total gate charge, Q_g is selected to minimize gate drive and switching losses. The R_{DS} resistance of MOSFET is usually an unimportant parameter because the switch conduction losses are not a significant part of the total converter losses at high operation frequency. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I_{Q(RMS)}^2$$

$$P_{SW} = \frac{I_L \times V_{SW}^2 \times C_{RSS} \times f_{SW}}{I_{GATE}}$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GATE} is gate drive output current, typically 500 mA. The MOSFET power rating and package should be selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

8. Rectifier Diode Selection

It suggest that use a Schottky diode as rectifier diode, because it provides the best efficiency due to the low forward voltage drop and near-zero reverse recovery time. Choose a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.

The current through the diode, I_D, is given by:

$$I_D = I_L \times (1 - D_{MAX})$$

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

9. Switch Current Sense Resistor

The switch current sense resistor, R_{IS}, is used for peak current mode control and to set the peak current limit. The value of R_{IS} is selected to protect the main switching MOSFET under fault conditions. The R_{IS} can be calculated based on peak inductor current, $I_{L(PK)}$, and switch current limit threshold, $V_{IS(LIMIT)}$.

$$R_{IS} = \frac{V_{IS(LIMT)}}{I_{L(PK)}}$$

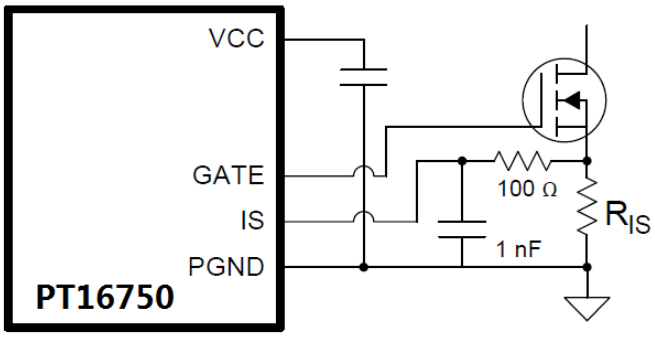


Figure 14. IS Input Filter

The use of a 1nF and 100Ω low-pass filter is optional. If used, the resistor value should be less than 500 Ω to limit its influence on the internal slope compensation signal.

10. Feedback Compensation

The open-loop response is the product of the modulator transfer function and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. The ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)}$$

Table 1 summarizes the expression for the small-signal model parameters.

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Buck	1	$\frac{1}{r_D \times C_{OUT}}$	/
Boost	$\frac{(1-D) \times V_O}{R_{IS} \times (V_O + (r_D \times I_{LED}))}$	$\frac{V_O + (r_D \times I_{LED})}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{L \times I_{LED}}$
Buck-Boost	$\frac{(1-D) \times V_O}{R_{IS} \times (V_O + (D \times r_D \times I_{LED}))}$	$\frac{V_O + (D \times r_D \times I_{LED})}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{D \times L \times I_{LED}}$

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 15) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 16, can be used to implement proportional and integral (PI) compensation and to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

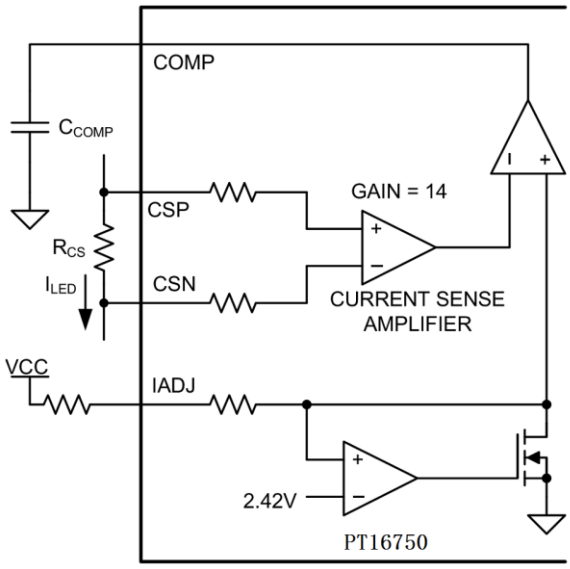


Figure 15. Integral Compensation

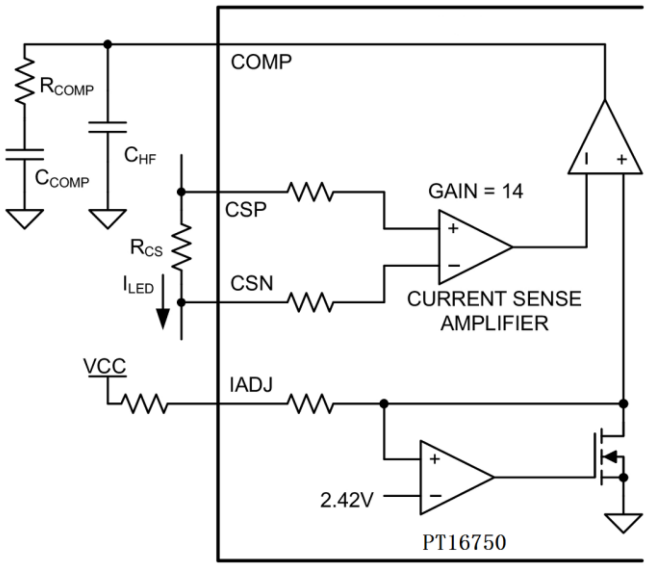


Figure 16. Proportional-Integral Compensation

The feedback transfer function is defined as follows.
Feedback transfer function with integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times C_{COMP}}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times (C_{COMP} + C_{HF})} \frac{(1 + s \times R_{COMP} \times C_{COMP})}{\left(1 + s \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)\right)}$$

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by placing the low-frequency zero an order of magnitude less than the crossover frequency. Use the following expressions to calculate the compensation network.
Buck with integral compensator:

$$C_{COMP} = \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP} = 8.75 \times 10^{-3} \times (\frac{R_{CS} \times G_0}{\omega_Z})$$

$$C_{HF} = \frac{C_{COMP}}{100}$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}}$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

11. Soft-Start

The time required for the LED current to reach the target setpoint is named the soft-start time (t_{SS}). Using a capacitor C_{SS} (from SS pin to GND) to set the required soft-start time, t_{SS}. C_{SS} can be calculated by following equation.

$$C_{SS} = 12.5 \times 10^{-6} \times t_{SS}$$

12. Overvoltage Protection

The controller includes a dedicated OVP pin which can be used for output overvoltage protection. For Boost and SEPIC topologies, as shown in Figure 9 and Figure 10, the overvoltage threshold is programmed using a resistor divider, R_{OV1} and R_{OV2}, from the output voltage (V_O) to GND. In the Buck-Boost or Buck configuration, as shown in Figure 11 and Figure 12, if the LEDs are referenced to a potential other than ground, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors.
The overvoltage turn-off threshold, $V_{O(OV)}$, is:
Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times (\frac{R_{OV1} + R_{OV2}}{R_{OV1}})$$

Buck and Buck-Boost:

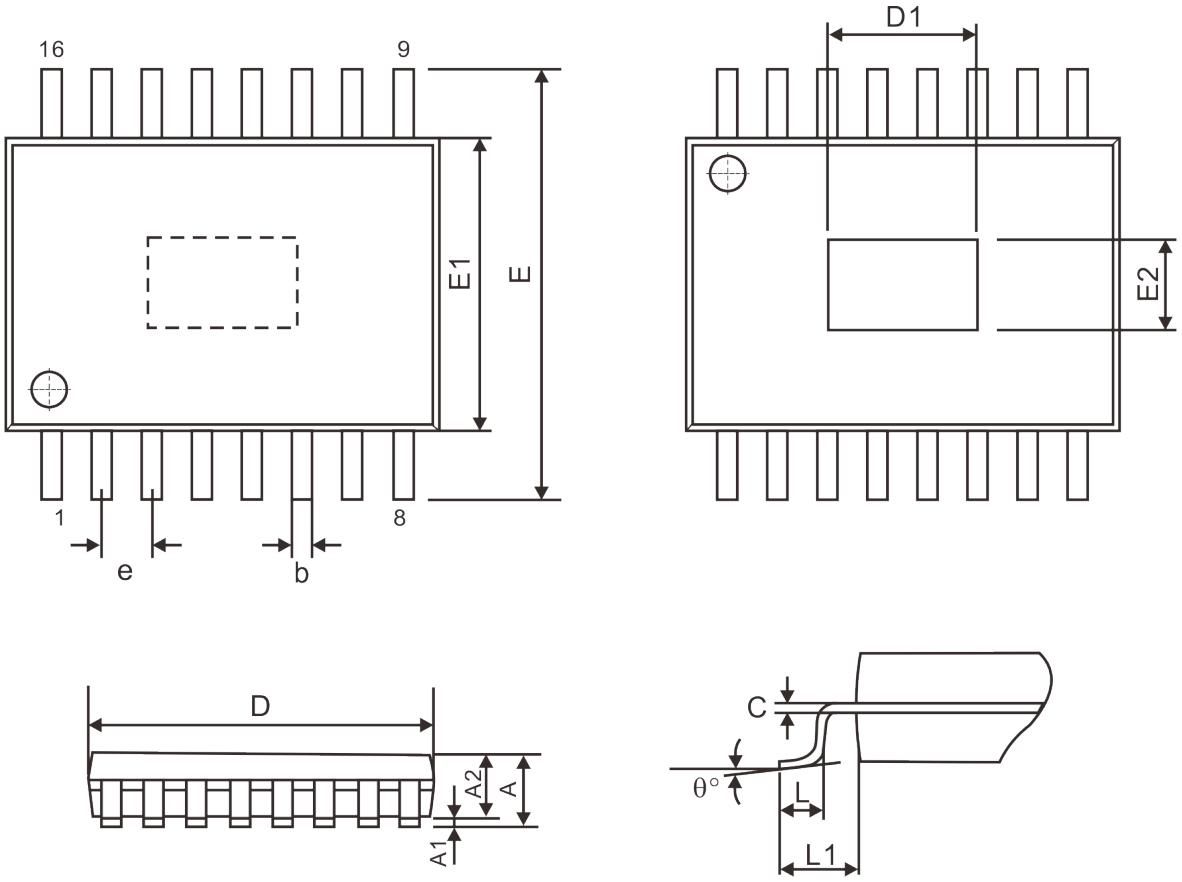
$$V_{O(OV)} = V_{OVP(THR)} \times \frac{R_{OV2}}{R_{OV1}} + 0.7$$

The overvoltage hysteresis, $V_{OV(HYS)}$ is:

$$V_{OV(HYS)} = I_{OVP(HYS)} \times R_{OV2}$$

PACKAGE INFORMATION

16-PIN, HTSSOP



Refer to JEDEC MO-153 AB/ABT (Thermally Enhanced Variations only)

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
e		0.65 BSC	
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E		6.4 BSC	
D1	2.40	-	3.00
E2	2.40	-	3.00
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	-	8°

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